2000 IEEE Microelectronics Reliability Qualification Workshop

Hot-Carrier Reliability of Transistors Fabricated by a 0.25-μm Fully-Depleted SOI CMOS Process

Udo Lieneweg and Anne Vandooren

Jet Propulsion Laboratory / California Institute of Technology
Mailstop 300-315, Pasadena CA 91109
Phone: 818-354-3444, Fax: 818-393-0045; Udo.Lieneweg@jpl.nasa.gov

Abstract

Fully depleted (FD) Silicon-On-Insulator (SOI) transistors are particularly susceptible to hot carrier effects because the thin silicon body has two closely spaced oxide interfaces. In the present work, the hot-carrier degradation of transistors fabricated by a 0.25-μm FD SOI CMOS process was investigated. The degradation of key transistor parameters under drain voltage stress and worst-case gate bias was observed as a function of time. The threshold voltage shift was analyzed with different back biases in order to separate front and back (buried) oxide degradation. A lifetime defined by a threshold voltage shift equal to one sigma of the original distribution was extracted as function of the drain voltage. Whereas the first batch of transistors showed a large sigma but a reasonable lifetime at 2 Volt, the other had a reasonable sigma but a lifetime of only 1 day at that voltage. It is shown that in the latter case the short lifetime is caused by poor properties of the buried oxide (here created by a SIMOX process). Therefore, SOI wafers must be characterized for their hot-carrier susceptibility.

Prefer oral but accept poster presentation.